AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

plural MOS transistors ~~which are disposed~~ in said substrate, each of said MOS transistors having a well with three diffusion regions therein, one of said three diffusion regions being connected to a power source or ground and two others of said three diffusion regions each being connected to a different respective one of a source and a drain, each of said MOS transistors also having a first gate electrode and a first gate insulating film between said first gate electrode and said substrate ~~and which include first gate insulating films~~; and

an MOS type varactor element ~~which is disposed~~ in said substrate, said MOS type varactor element having a second conductivity type well with two second conductivity type diffusion regions therein that are connected to a common well terminal, said MOS type varactor element also having a second gate electrode and ~~which includes~~ a second gate insulating film between said second gate electrode and said substrate, ~~a gate electrode and a second conductivity type well,~~ wherein ~~said~~

~~second gate insulating film,~~ said gate electrode and said common well terminal have a variable voltage therebetween that corresponds to a variable capacitance between said second gate electrode and said second conductivity type well ~~second conductivity type well are a variable capacitor~~,

a thickness of said second gate insulating film being thinner than the thinnest gate insulating film among said first gate insulating films of said MOS transistors.

2. (original) A semiconductor integrated circuit device according to Claim 1, wherein a maximum gate voltage applied to said MOS type varactor element is lower than a maximum gate voltage applied to said MOS transistors.

3. (original) A semiconductor integrated circuit device according to Claim 1, wherein said substrate is a semiconductor substrate.

4. (original) A semiconductor integrated circuit device according to Claim 2, wherein said substrate is a semiconductor substrate.

5. (canceled)

6. (currently amended) The device of claim [[5]]1, wherein said second gate insulating film of said varactor and said first gate insulating films of said plural MOS transistors are at a same level of the device.

7. (currently amended) The device of claim [[5]]1, wherein the thickness of said second gate insulating film of said

varactor is about three quarters of a thickness of said first gate insulating films of said plural MOS transistors.

8. (currently amended) The device of claim 7, wherein the thickness of said second gate insulating film of said varactor is about 6 nm and the thickness of said first gate insulating films of said plural MOS transistors is about 8 nm.

9-12. (canceled)

13. (previously presented) The device of claim 1, wherein said MOS transistors are spaced from said varactor element and include an N-channel MOS transistor and a P-channel MOS transistor.

14-15. (canceled)

16. (currently amended) The semiconductor integrated circuit device according to claim [[15]]1, wherein said two second conductivity type diffusion regions ~~layer~~ of said MOS type varactor element [[is]] are adjacent to ~~a side~~ opposing sides of said second gate electrode.

17-22. (canceled)

23. (new) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors disposed in said substrate and including first insulating films; and

an MOS type varactor element disposed in said substrate and including a second insulating film, a conductive electrode and a second conductivity type well,

wherein said second insulating film, said conductive electrode and said second conductivity type well form a variable capacitor,

wherein a thickness of said second insulating film is thinner than that of the thinnest insulating film among said first insulating films of said MOS transistors,

wherein first and second diffusion layers are provided at both sides of said conductive electrode, and said first and second diffusion layers are connected to a common terminal through first and second wiring line respectively.

24. (new) The semiconductor integrated circuit device according to claim 23, wherein a variable capacitance is formed between said conductive electrode and said second conductivity type well, and said variable capacitance is response to a voltage between said conductive electrode and said second conductivity type well.

25. (new) The semiconductor integrated circuit device according to claim 23, wherein maximum gate voltage applied to said MOS type varactor element is lower than a minimum gate voltage applied to said MOS transistors.

26. (new) The semiconductor integrated circuit device according to claim 23, wherein said MOS transistors include an N-channel MOS transistor and P-channel MOS transistor.

27. (new) The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are second conductivity type diffusion layers.

28. (new) The semiconductor integrated circuit device according to claim 27, wherein said common terminal supplies with a potential of said second conductivity type well through said first and second diffusion layers.

29. (new) The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are first conductivity type diffusion layers.

30. (new) The semiconductor integrated circuit device according to claim 29, wherein said MOS type varactor element further comprises a third diffusion layer disposed in said second conductivity type well, said third diffusion layer is connected to a terminal different from said common terminal through a third wiring line.

31. (new) The semiconductor integrated circuit device according to claim 30, wherein said third diffusion layer is a second conductivity type diffusion layer.

32. (new) The semiconductor integrated circuit device according to claim 31, wherein said terminal supplies with a

potential of said second conductivity type well through said third diffusion layer.

33. (new) The semiconductor integrated circuit device according to claim 32, wherein said common terminal supplies said first and second diffusion layers with a ground potential.

34. (new) The semiconductor integrated circuit device according to claim 23, wherein a thickness of said second insulating film of said MOS type varactor element is about three quarters of a thickness of first insulating films of said MOS transistors.

35. (new) The semiconductor integrated circuit device according to claim 34, wherein the thickness of said second insulating film of said MOS type varactor element is about 6 nm and the thickness of first insulating films of said MOS transistors is about 8 nm.